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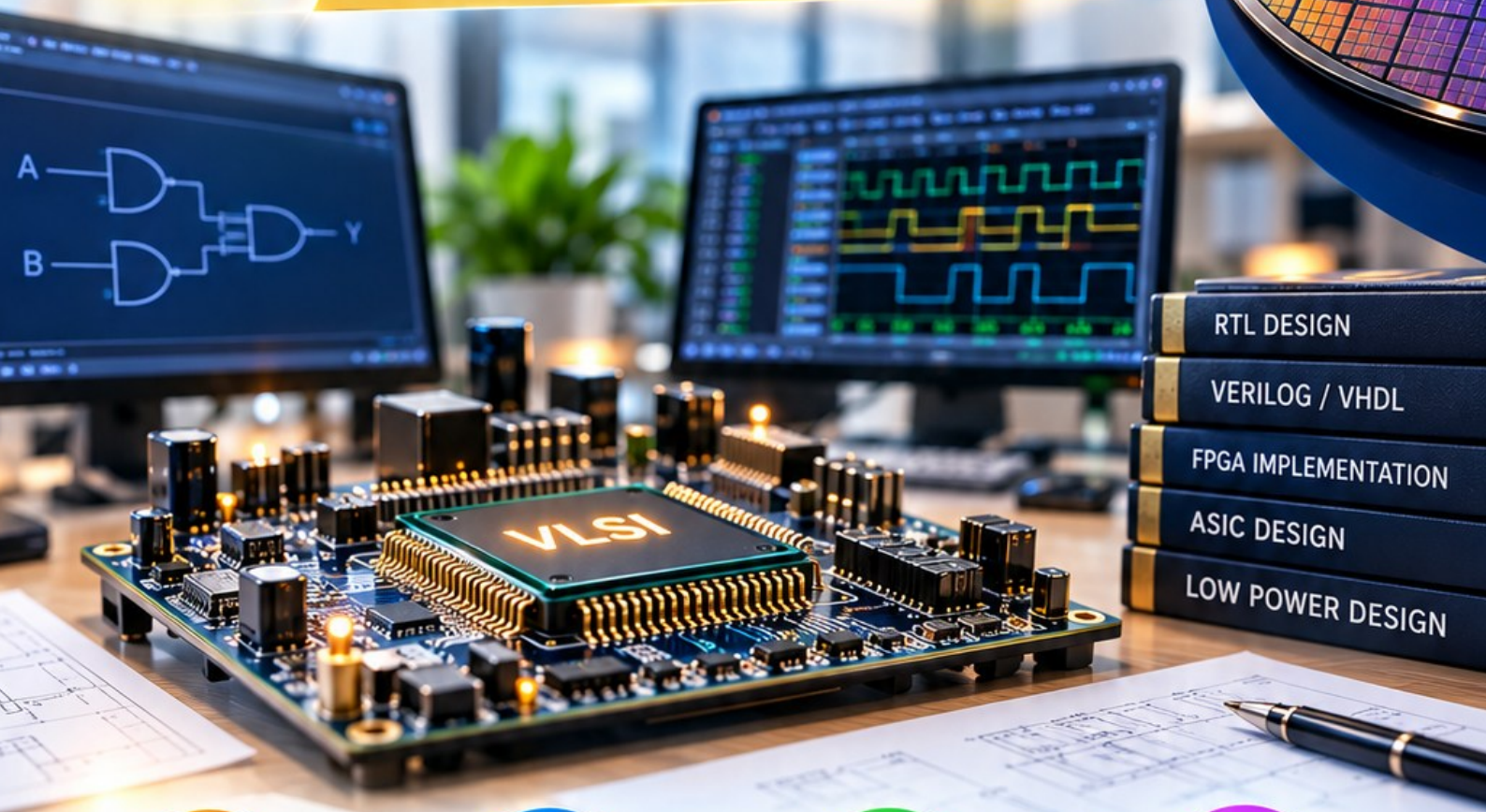
ISO9001:2015 Certified
TELANGANA | ANDHRA PRADESH

18 YEARS OF EXCELLENCE

DESIGN
SIMULATE
ANALYZE
IMPLEMENT

# VLSI PROJECTS LIST




**DIGITAL DESIGN**

**VERILOG / VHDL**

**SIMULATION & VERIFICATION**

**FPGA / ASIC IMPLEMENTATION**

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SILICON SOLUTIONS FOR A SMARTER TOMORROW

# VLSI PROJECT TITLES LIST- 2027

| S.NO | P.CODE | Project Title Name |
|---|---|---|
| 1 | V2601 | Design and Implementation 8bit ALU Verilog HDL Vivado |
| 2 | V2602 | Advanced Encryption Standard Algorithm With Optimal S-Box and Automated Key Generation |
| 3 | V2603 | Design and Verification of DDR SDRAM Memory Controller Using SystemVerilog |
| 4 | V2604 | Fast Binary Counters and Compressors Generated by Sorting Network |
| 5 | V2605 | Adaptive Hold Logic for Aging-Aware Reliable Multiplier Design. |
| 6 | V2606 | Efficient Systolic Array Architecture Design for DWT. |
| 7 | V2607 | Design of a Lightweight RISC-V Processor with Custom AI Acceleration Instructions |
| 8 | V2608 | Design and Verification of a Secure RISC-V Processor with Hardware Isolation |
| 9 | V2609 | Hardware Implementation of a RISC-V Matrix Processing Extension for AI Workloads |
| 10 | V2610 | Design and Verification of a Secure Hardware Key Generation Module |
| 11 | V2611 | Design and Verification of a Low-Power Pipelined ALU Using SystemVerilog |
| 12 | V2612 | SystemVerilog-Based Design of an Error Detection and Recovery Architecture |
| 13 | V2613 | Design of a Configurable Digital FIR Filter Using SystemVerilog |
| 14 | V2614 | 8T SRAM Based In-Memory DAC for AI acceleration |
| 15 | V2615 | An Efficient Feed-forward Neural Network Implementation Based on FPGA |
| 16 | V2616 | Design and Implementation of a 3-stage RISC-V CPU |
| 17 | V2617 | Design and Implementation of a FIR by using fpga |
| 18 | V2618 | Design and Verification of APB with UART at IP |
| 19 | V2619 | Design of a Digital Temperature Sensor Interface for Smart VLSI Systems |
| 20 | V2620 | Design of Compact Modified Radix-4 |
| 21 | V2621 | FPGA-Based_Improved_Sobel_Operator_Edge_Detection |
| 22 | V2622 | Implementation and Analysis of a 5-Stage Pipelined RISC-V Processor with Forwarding Unit |
| 23 | V2623 | ProNoC: A Low Latency Network-on-Chip Based Many-Core System-on-Chip Prototyping Platform |
| 24 | V2624 | FPGA Implementation of an Intelligent Traffic Light Controller (I-TLC) in Verilog |
| 25 | V2625 | EMPOWERING COMMUNICATION FPGA –based Morse Code system for differently - abled individuals |
| 26 | V2626 | Design and Simulation of Single Master Single Slave Serial Peripheral Interface (SPI) with Adaptive Baud Rate Using Verilog |
| 27 | V2627 | Design And Verification Of Uart Using verilog hdl |
| 28 | V2628 | Optimal Implementation Of Uart-Spi Interface In Soc |
| 29 | V2629 | FPGA Based Secure Electronic Voting Machine Using Fingerprint Authentication |
| 30 | V2630 | An FPGA application of home security code using verilog |
| 31 | V2501 | Design and Implementation 8bit ALU Verilog HDL Vivado |
| 32 | V2502 | Advanced Encryption Standard Algorithm With Optimal S-Box and Automated Key Generation |
| 33 | V2503 | Design and Verification of DDR SDRAM Memory Controller Using SystemVerilog |
| 34 | V2504 | Fast Binary Counters and Compressors Generated by Sorting Network |
| 35 | V2505 | Adaptive Hold Logic for Aging-Aware Reliable Multiplier Design. |
| 36 | V2506 | Efficient Systolic Array Architecture Design for DWT. |
| 37 | V2507 | Design of a Lightweight RISC-V Processor with Custom AI Acceleration Instructions |
| 38 | V2508 | Design and Verification of a Secure RISC-V Processor with Hardware Isolation |
| 39 | V2509 | Hardware Implementation of a RISC-V Matrix Processing Extension for AI Workloads |
| 40 | V2510 | Design and Verification of a Secure Hardware Key Generation Module |
| 41 | V2511 | Design and Verification of a Low-Power Pipelined ALU Using SystemVerilog |

| | | |
|---|---|---|
| 42 | V2512 | SystemVerilog-Based Design of an Error Detection and Recovery Architecture |
| 43 | V2513 | Design of a Configurable Digital FIR Filter Using SystemVerilog |
| 44 | V2514 | 8T SRAM Based In-Memory DAC for AI acceleration |
| 45 | V2515 | An Efficient Feed-forward Neural Network Implementation Based on FPGA |
| 46 | V2516 | Design and Implementation of a 3-stage RISC-V CPU |
| 47 | V2517 | Design and Implementation of a FIR by using fpga |
| 48 | V2518 | Design and Verification of APB with UART at IP |
| 49 | V2519 | Design of a Digital Temperature Sensor Interface for Smart VLSI Systems |
| 50 | V2520 | Design of Compact Modified Radix-4 |
| 51 | V2401 | FPGA-Based_Improved_Sobel_Operator_Edge_Detection |
| 52 | V2402 | Implementation and Analysis of a 5-Stage Pipelined RISC-V Processor with Forwarding Unit |
| 53 | V2403 | ProNoC: A Low Latency Network-on-Chip Based Many-Core System-on-Chip Prototyping Platform |
| 54 | V2404 | FPGA Implementation of an Intelligent Traffic Light Controller (I-TLC) in Verilog |
| 55 | V2405 | EMPOWERING COMMUNICATION FPGA –based Morse Code system for differently - abled individuals |
| 56 | V2406 | Design and Simulation of Single Master Single Slave Serial Peripheral Interface (SPI) with Adaptive Baud Rate Using Verilog |
| 57 | V2407 | Design And Verification Of Uart Using verilog hdl |
| 58 | V2408 | Optimal Implementation Of Uart-Spi Interface In Soc |
| 59 | V2409 | FPGA Based Secure Electronic Voting Machine Using Fingerprint Authentication |
| 60 | V2410 | An FPGA application of home security code using verilog |
| 61 | V2411 | Recursive Approach to the Design of a Parallel Self-Timed Adder |
| 62 | V2412 | Low-Power and Area-Efficient Shift Register Using Pulsed Latches |
| 63 | V2413 | High Speed Convolution And Deconvolution Algorithm Based On Ancient Indian Vedic Mathematics |
| 64 | V2414 | Area-Delay Efficient Binary Adders in QCA |
| 65 | V2415 | Design and Simulation of Power Efficient Traffic Light Controller (PTLC) |
| 66 | V2416 | Novel High Speed Vedic Mathematics Multiplier using Compressors |
| 67 | V2417 | VLSI implementation of Fast Addition using Quaternary Signed Digit Number System |
| 68 | V2418 | Design and Implementation of 32 Bit Unsigned Multiplier Using CLAA and CSLA |
| 69 | V2419 | Implementation of RNG in FPGA using Efficient Resource Utilization |
| 70 | V2420 | Implementation of High Speed Low Power Combinational and Sequential Circuits using Reversible logic |
| 71 | V2421 | A High Speed Binary Floating Point Multiplier Using Dadda Algorithm |
| 72 | V2422 | A novel approach to realize Built-in-self-test(BIST) enabled UART using VHDL |
| 73 | V2423 | The design of high performance Barrel Integer Adder |
| 74 | V2424 | Implementation of Power Efficient Vedic Multiplier |
| 75 | V2425 | Design and Implementation of Carry Select Adder without Using Multiplexers |

# New Zen Infotech

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